REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-4 and 6-35 remain in the application. Claim 5 has been cancelled. Claims 20-35 have been withdrawn. It is noted that there are two claims numbered 30. The Examiner is requested to renumber claims 30-35 as 30-36.

In the section entitled "Claim Objections" on page 2 of the above-identified Office action, claims 5 and 6 have been objected to because claims 5 and 6 are identical. Claim 5 has been cancelled.

In the section entitled "Claim Rejections - 35 USC § 103" on pages 2-4 of the above-mentioned Office action, claims 1-4, 7-9, and 11-19 have been rejected as being unpatentable over Barret et al. (US Pat. No. 5,780,895) in view of Nandakumar et al. (US Pat. No. 5,296,725) under 35 U.S.C. § 103(a); claims 5 and 10 have been rejected as being unpatentable over Barret et al., Nandakumar et al. and further in view of Liao et al. (US Pat. No. 6,359,309) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and

the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a region of the second conductivity type being incorporated into said substrate, reaching to said first side, and electrically connecting to said second gate of said further MOS cells, said region having a potential floating relative to the potential of the first and second source regions of said MOS cells and further MOS cells.

The subject matter of the invention of the instant application is a vertical semiconductor component (see Fig. 2) with a semiconductor substrate (1) of a first conductivity type, a first side (I) of which is covered by an insulating layer (8) and a second side (II) of which terminates at a more highly doped layer (2) of the first conductivity type. MOS cells (M, SU) are formed in the semiconductor substrate (1) in the region of the first side (I), each of which has a well (4, 4') of a second conductivity type, a source zone (5, 5') of the first conductivity type embedded in the well, and a source contact (6, 6') contacting the source zone (5, 5'). The source contact reaches the source zone (5, 5') through the insulating layer (8). The MOS cells (M, SU) further have

gate-electrodes (7, 7'), which are disposed on a side of the insulating layer (8) remote from the substrate (1). The MOS cells are divided into two groups. The source contacts (6) of the first group (M) of the MOS cells are electrically insulated from the source contacts (6') of the second group (SU) of the MOS cells.

The component according to the invention of the instant application further includes a semiconductor zone (11) of the second conductivity type that is disposed in the semiconductor substrate (1), which reaches to the first side (I) and is electrically connected with the gate electrode (7') of the second group (SU) of the MOS cells.

Barret et al. describe a vertical semiconductor component with a semiconductor substrate 0 of a first conductivity type, on one side of which a more highly doped semiconductor layer 11 of the first conductivity type is attached (see Fig 3). First MOS cells are disposed in the region of the side of the semiconductor substrate 0 remote from the more highly doped layer 11, each of which has a well 5 of a second conductivity type, a source zone 2 of the first conductivity type embedded in the well 5, a source contact 3, and a gate electrode 6. Fig. 3 of Barret et al. shows a further MOS cell with a well 45 of the second conductivity type, in which a source zone 42

of the first conductivity type is embedded. This source zone 42 is contacted through a source electrode 43. All MOS cells in Barret et al. have a common gate electrode 6.

In contrast to the semiconductor component according to claim 1 of the instant application, the component of Barret et al. does not have a semiconductor zone of the second conductivity type in the semiconductor substrate, which contacts the gate electrode 6. This kind of semiconductor zone disposed in the semiconductor substrate and contacting the gate electrode is also not disclosed in Nandakumar et al.

Nandakumar et al. describe a semiconductor component with a semiconductor substrate 16 of a first conductivity type, in which MOS cells are disposed (see Fig. 3). A semiconductor zone 33 of a second conductivity type, which has a terminal contact 55, is disposed in the semiconductor substrate 16. In contrast to the semiconductor component according to claim 1 of the instant application, the terminal contact 55 is not connected to the gate electrodes 38, 46, 54 of the MOS cells. These gate electrodes 38, 46, 54 are jointly connected to a gate potential V_{GATE}. In contrast, the terminal 55 of the semiconductor zone 33 of the second conductivity type is connected to a cathode of the component (see column 8, lines 46-47 of Nandakumar et al.).

Contrary to the opinion of the Examiner, a combination of the components of Barret et al. and Nandakumar et al. would not lead to a semiconductor component according to claim 1 of the instant application. It is noted that Barret et al. describe a vertical MOS transistor, whereas Nandakumar et al. describe a vertical thyristor, which distinguishes itself by the fact that a semiconductor layer 14 doped complementarily to the semiconductor substrate 16 is applied on the semiconductor substrate 16 in the region of the backside of the component. Since the components of the cited references describe completely different functional principles, a person skilled in the art would not combine Barret et al. and Nandakumar et al. with each other.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-19 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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